JVA Internships

Professional Training Programs

Analog Layout

Master Industry-Level Analog Layout Design

Learn practical backend layout techniques, physical verification concepts,

What You Will Learn

- CMOS Layout Fundamentals
- Floorplanning Techniques
- Routing Concepts
- DRC & LVS Verification
- Matching Techniques
- Power Planning Basics
- Layout Optimization
- Physical Verification Flow

Program Highlights

- Tool-Based Practical Sessions
- Real Chip Layout Practices
- Backend Design Workflow
- Hands-On Lab Training
- Mentor Guidance

Who can Apply?

- ECE / EEE Students
- B.Tech / M.Tech Graduates
- VLSI Enthusiasts
- Freshers Looking for Semiconductor Careers

Why Choose This Program?

- Learn Industry Layout Standards
- Practical Backend VLSI Training
- Exposure to Real Chip Design Concepts
- Strong Foundation in Analog Layout
- Career Support & Guidance

INTERNSHIP OUTCOMES

- Understand complete layout flow
- Perform DRC & LVS verification
- Work on routing and floorplanning tasks
- Handle layout implementation basics
- Prepare for Analog Layout interviews

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